Amendments t th Claims

LISTING OF CLAIMS

Claims 1-25 (canceled)

26. (original) A method for fabricating a semiconductor component comprising:

providing a semiconductor die comprising an electrically insulating layer and a plurality of die contacts;

forming a first electrode on the electrically insulating layer in electrical communication with a first die contact;

forming a dielectric layer on the first electrode;

forming a second electrode on the dielectric layer in electrical communication with a second die contact;

forming a first terminal contact on the die in electrical communication with the first electrode;

forming a second terminal contact on the die in electrical communication with the second electrode; and

forming a protective layer on the die encapsulating the first electrode, the dielectric layer and the second electrode.

27. (original) The method of claim 26 wherein the forming the first electrode step comprises patterning a first redistribution layer on the die.

28. (original) The method of claim 26 wherein the forming the second electrode step comprises patterning a second redistribution layer on the die.

29. (original) The method of claim 26 wherein the first die contact comprises a ground contact for the die.

30. (original) The method of claim 26 wherein the second die contact comprises a power contact for the die.

31. (original) The method of claim 26 wherein the die contacts comprise bond pads.

32. (original) The method of claim 26 wherein the electrically insulating layer comprises a passivation layer.

33. (original) The method of claim 26 wherein the terminal contacts comprise bumps or balls in a grid array.

34. (original) A method for fabricating a semiconductor component with an on board capacitor comprising:

providing a semiconductor die comprising a plurality of die contacts;

forming a first redistribution layer on the die;

patterning the first redistribution layer to form a first electrode of the capacitor in electrical communication with a first die contact;

forming a dielectric layer of the capacitor on the first electrode;

forming a second redistribution layer on the die and on the dielectric layer; and

patterning the second redistribution layer to form a second electrode of the capacitor in electrical communication with a second die contact.

35. (original) The method of claim 34 further comprising forming a first terminal contact on the die in electrical communication with the first electrode.

36. (original) The method of claim 34 further comprising forming a second terminal contact on the die in electrical communication with the second electrode.

37. (original) The method of claim 34 further comprising forming a protective layer on the die encapsulating the first electrode, the dielectric layer and the second electrode.

38. (original) The method of claim 34 wherein the first die contact comprises a ground contact and the second die contact comprises a power contact.

39. (original) A method for fabricating a semiconductor component with an on board capacitor comprising:

providing a semiconductor die comprising a plurality of integrated circuits and a plurality of die contacts in electrical communication with the integrated circuits;

forming an on board capacitor on die by forming a first electrode on the die in electrical communication with a ground die contact, a dielectric layer on the first electrode, and a second electrode on the dielectric layer in electrical communication with a power die contact; and

forming a plurality of terminal contacts on the die in electrical communication with the die contacts, including a ground terminal contact in electrical communication with the first electrode, and a power terminal contact in electrical communication with the second electrode.

40. (original) The method of claim 39 further comprising forming a protective layer on the die encapsulating the capacitor.

41. (original) The method of claim 39 wherein the terminal contacts comprise bumps or balls in a grid array.

42. (original) The method of claim 39 wherein forming the first electrode comprises patterning a first redistribution layer for the die.

43. (original) The method of claim 39 wherein forming the second electrode comprises patterning a second redistribution layer for the die.

44. (original) The method of claim 39 further comprising forming a ground conductor on the die in electrical communication with the ground die contact and the first electrode.

45. (original) The method of claim 39 further comprising forming a plurality of conductors on the die in electrical communication with the die contacts and the terminal contacts comprising portions of a redistribution layer.

46. (original) The method of claim 39 wherein the component comprises a package.

47. (original) The method of claim 39 wherein the die is contained on a semiconductor wafer comprising a plurality of dice identical to the die.

48. (original) A method for fabricating a semiconductor component with an on board capacitor comprising:

providing a semiconductor wafer containing a semiconductor die;

forming a first redistribution layer on the wafer;

forming a first electrode of the capacitor by patterning the first redistribution layer;

forming a dielectric layer on the first electrode;

forming a second redistribution layer on the wafer;

forming a second electrode on the dielectric layer by patterning the second redistribution layer; and

forming a protective layer on the wafer encapsulating the first electrode, the dielectric layer and the second electrode.

49. (original) The method of claim 48 further comprising singulating the die from the wafer.

50. (original) The method of claim 48 further comprising forming a plurality of terminal contacts on the die including a ground terminal contact in electrical communication with the first electrode and a power terminal contact in electrical communication with the second electrode.

Claims 51-59 (canceled)